## Simulation and experimental characterization of Out-of-SOA events of Power Semiconductor devices

## Prof. Andrea Irace, Ph.D, University of Naples Federico II, Italy



Prof. Andrea Irace received the Laurea and Ph.D. degrees in Electronic Engineering from the University of Naples Federico II, Naples, Italy, in 1994 and 1998, respectively. He has been a *visiting scientist* at the Delft University of Technologies. He is currently employed as an Associate Professor of Electronics. His research interests include power semiconductor devices, especially in the fields of device characterization and modelling of highly stressful events. Professor Irace has authored or co-authored more than 150 papers published in international journals or conferences, has been a member of the Technical Program Committee of the IEEE International Symposium on Power Semiconductor Devices and ICs and is a regular reviewer for International Journals and Conferences.

## Abstract

As power semiconductor devices becomes widely used in environments where their reliability over many years of operation is a mandatory need (i.e. automotive industry), the knowledge of the working condition that may lead to their degradation or even field failure becomes of paramount importance. Out-of-SOA events, such as short circuit conduction and avalanche operation might happen during the normal life of a power device even in the most carefully designed circuit configurations. For this reason, their understanding, modeling, simulation and characterization have become a strong requirement in both industrial and academic communities. While the knowledge of device behavior within the SOA boundaries is well understood and correctly modeled at any level (physical TCAD, SPICE, behavioral etc.), when the device operates close or outside the SOA boundaries, these models start to show their limits as they do not take into account spatial or volume effects such as current filamentation which may be the onset of device degradation and failure. Further insight and understanding of these phenomena can be gained from experiments where unusual behavior in the current and voltage waveforms of the device under test can point the investigation toward the inner behavior of the power device itself. The lecture will address these topics with great detail, with a special focus on the compact electro-thermal modeling of power semiconductor devices and the description non-conventional characterization techniques, such as Infrared Thermography, for the evaluation of uneven current distribution over the device area during a stressful out-of-SOA event.